WHAT IS CLAIMED IS:

1. A graphic processor, comprising:

a first interface for receiving an externally-input graphics command;

a second interface for performing a data transfer operation between the graphic processor and a work memory;

a data bus for transferring data between the first interface and the second interface;

a display data generation section for receiving a graphics command from the data bus, generating display data by decoding the graphics command, and outputting the generated display data to the data bus;

an image display section for receiving the display data from the data bus and displaying an image on a display device; and

a bus control section for monitoring a status of use of the data bus and controlling a right to use the data bus,

wherein the bus control section sets a priority for each data transfer operation along the data bus and controls the right to use the data bus according to the set priorities.

2. The graphic processor of claim 1, wherein the bus control section sets a priority for each of at least the following data transfer operations: a data transfer operation of transferring an externally-input graphics command to the work memory; a data transfer operation of supplying a graphics command from the work memory to the display data

generation section; and a data transfer operation of supplying display data from the work memory to the image display section.

3. The graphic processor of claim 1, wherein the bus control section is configured so that a setting of the priorities of data transfer operations can be changed dynamically.

4. The graphic processor of claim 3, further comprising:

a pre-decoding section for pre-decoding a graphics command transferred during a data transfer operation of transferring an externally-input graphics command to the work memory; and

a processing amount estimating section for estimating a data processing amount at the display data generation section based on a result of the pre-decoding by the pre-decoding section,

wherein the bus control section changes the priorities of the data transfer operations according to the data processing amount estimated by the processing amount estimating section.

5. The graphic processor of claim 4, wherein when the estimated data processing amount per a predetermined period of time exceeds a predetermined amount, the bus control section sets the priority of a data transfer operation of supplying a graphics command from the work memory to the

display data generation section to be higher than the priority of a data transfer operation of transferring an externally-input graphics command to the work memory.

6. The graphic processor of claim 3, further comprising a memory monitor for monitoring an amount of data of graphics commands stored in the work memory,

wherein the bus control section changes the priorities of the data transfer operations according to the data amount monitored by the memory monitor.

7. The graphic processor of claim 6, wherein when the monitored data amount is smaller than a predetermined amount, the bus control section sets the priority of a data transfer operation of transferring an externally-input graphics command to the work memory to be higher than the priority of a data transfer operation of supplying a graphics command from the work memory to the display data generation section.

8. The graphic processor of claim 3, wherein:

the first interface is connected to an external bus which is provided external to the graphic processor;

an external bus monitor for monitoring an amount of data being transferred along the external bus is connected to the external bus; and

the bus control section changes the priorities of the data transfer operations along the data bus according to the amount of data being transferred which is monitored by the external bus monitor.

9. The graphic processor of claim 1, wherein:

the display data generation section includes a graphics command storing section for temporarily storing a graphics command which is input through the data bus, and a decoding section for decoding a graphics command which is output from the graphics command storing section;

the graphics command storing section includes first data storing means and second data storing means, writes graphics commands into selected one of the first and second data storing means in a predetermined address order, and reads out graphics commands from selected one of the first and second data storing means in a predetermined address order; and

when a reading address in one of the first and second data storing means from which graphics commands are being read out matches a predetermined check address, the graphics command storing section starts writing new graphics commands into the one of the first and second data storing means.

10. A graphic processing system, comprising:

the graphic processor of claim 1;

an external bus connected to the first interface of the graphic processor;

a CPU and a memory which are connected to the external bus;

a work memory connected to the second interface of the graphic processor; and

a display device connected to the image display section of the graphic processor.

11. A graphic processor, comprising:

a first interface for receiving an externally-input graphics command;

a second interface for performing a data transfer operation between the graphic processor and a work memory;

a data bus for connecting the first interface with the second interface;

a display data generation section for receiving a graphics command from the data bus, generating display data by decoding the graphics command, and outputting the generated display data to the data bus; and

an image display section for receiving the display data from the data bus and displaying an image on a display device, wherein:

the display data generation section includes a graphics command storing section for temporarily storing a graphics command which is input through the data bus, and a decoding section for decoding a graphics command which is output from the graphics command storing section;

the graphics command storing section includes first data storing means and second data storing means, writes graphics commands into selected one of the first and second data storing means in a predetermined address order, and reads out graphics commands from selected one of the first

and second data storing means in a predetermined address order; and

when a reading address in one of the first and second data storing means from which graphics commands are being read out matches a predetermined check address, the graphics command storing section starts writing new graphics commands into the one of the first and second data storing means.